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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,772	12/08/2003	Seung-Hyun Rhee	50432-616	1077

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McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
DAHIMENE, MAHMOUD	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 09/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/728,772	RHEE ET AL.	
	Examiner	Art Unit	
	Mahmoud Dahimene	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f)

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/8/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

96DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 6, 7 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 6, SilK is a trademark name for a low-k material. If the trademark or trade name is used in a claim as a limitation to identify or describe a particular material or product, the claim does not comply with the requirements of the 35 U.S.C. 112, second paragraph. Ex parte Simpson, 218 USPQ 1020 (Bd. App. 1982). The claim scope is uncertain since the trademark or trade name cannot be used properly to identify any particular material or product. In fact, the value of a trademark would be lost to the extent that it became descriptive of a product, rather than used as an identification of a source or origin of a product. Thus, the use of a trademark or trade name in a claim to identify or describe a material or product would not only render a claim indefinite, but would also constitute an improper use of the trademark or trade name.

As to claims 7 and 10, they are dependant on claim 6.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uzoh et al. (US 6413854) and further in view of Gaw et al. (US 6303464).

Applicants are claiming a method of forming an interlevel dielectric layer, comprising the steps forming a polymer sacrificial ILD on a substrate, forming metallization structures within the polymer sacrificial ILD, etching back the polymer sacrificial ILD, non-conformally depositing dielectric material as an ILD layer over the substrate and the metallization structures so as to form air gaps in the ILD layer between at least some of the metallization structures.

Uzoh discloses a method of forming a multi-level metal (relating to applicant's claim 1) structure/ an interconnect (relating to applicant's claim 11) structure (column 9, lines 9-25). The process involves: depositing a first dielectric material (13) on a substrate (11) (column 9, line 11) (figures 5-13), patterning the first dielectric material (column 9, line 12) (figure 6); depositing at least one metal (19) in openings in the patterned first dielectric and on the patterned first dielectric material, removing portions of the at least one metal at least in a region above an upper surface of the first dielectric material (column 9, lines 16-19) (figures 8-9), removing the first dielectric material

(column 9, line 20) (figure 12), and providing a second dielectric material (43) in place of the first dielectric material (column 9, line 21) (figure 13).

A difference is noted between applicant's claims and the reference of Uzoh. Uzoh fails to teach a step corresponding to the applicant's step consisting of depositing a non-conformal dielectric material in claim 1.

Gaw teaches a similar semiconductor manufacturing process for reducing the interconnect system capacitance through enclosed voids in a dielectric layer. See abstract. Gaw discloses that after removal of the first dielectric, which could be a Fluoropolymer, deposition of a non-conformal dielectric over the substrate on a metal layer, and on the trenches between interconnects such that voids or air gaps are formed, is desirable because air voids between interconnects lower the effective dielectric constant between metal lines, reducing capacitance, and cross-talk effects (column 1, lines 14-34).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the process of Uzoh to include the step of depositing a non-conformal dielectric layer allowing the formation of air gaps in the second dielectric between metal lines because Gaw illustrates that introducing air gaps between metal lines is desirable because it results in the production of a chip with less capacitance delay and interconnect cross-talk. One of ordinary skill in the art would have been motivated to include air gaps in the second dielectric in order to obtain less capacitance and cross-talk effects resulting in the capability of manufacturing a faster chip (Gaw; column 1, lines 14 to column 2, line 32).

5. As to claim 2, Uzoh includes copper as a typical interconnect fill (column 4, line 44).

6. As to claim 3, Uzoh describes a cap layer over the copper (column 4, line 54).

7. As to claim 4, Uzoh discloses that the cap layer on top of the copper may protect the metal during the first dielectric etch (column 5, line 24).

8. As to claim 5, Uzoh includes Ta as a cap layer (column 4, line 65).

9. As to claim 6, Uzoh includes SilK as a first dielectric material (column 3, line 39).

10. As to claim 7, Uzoh does not explicitly disclose using SiO_2 / SiOF as materials for the ILD layer, Gaw discloses SiO_2 or SiOF as materials for the ILD layer (column 4, line 20).

The characteristics of SiO_2 materials for non-conformal deposition are well known in the art (Wolf et al. (Volume1, page 183)), allowing for a reliable method to include voids (or air gaps). Also, SiOF has a lower k value (Wolf et al. (Volume 4, page 654)) and similar mechanical properties as SiO_2 consequently it is also desirable for applications that require low-k dielectrics.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the process of Uzoh by selecting SiO_2 or SiOF

as a second ILD because Gaw discloses a method for reducing capacitance and cross-talk effects between metal interconnect lines by including voids or air gaps by using SiO_2 or SiOF. One of ordinary skill in the art would have been motivated to include SiO_2 or SiOF materials as the second dielectric because the use of these materials allows formation of air gaps which in turns lowers the k value between metal lines.

11. As to claims 8, 9 and 16, Uzoh discloses a method, wherein, a mask is not needed to etch back the sacrificial ILD layer (which could be a polymer), (column 9, lines 9-24), making it a self-aligned process.

12. As to claims 10 and 14, both Uzoh and Gaw include the possibility of using any dielectric material having a low dielectric constant (Uzoh, column 8, line 5) such as porous silica, etc.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the process of Uzoh to include any ultra low k dielectric (provided the material meets all manufacturing and reliability requirements) as a second ILD, as taught by Gaw (column 1, line 45) because it is desirable to lower the dielectric k value between metal lines to reduce capacitance and cross-talk effects. One of ordinary skill in the art would have been motivated to include ultra low k materials as the second dielectric in order to obtain a faster chip (Wolf et al. (Volume 4, page 663).

13. As to claim 12, Uzoh fails to disclose a second dielectric layer comprising voids (or air gaps) between consecutive metal lines, Gaw discloses a second dielectric layer non-conformally deposited over the metal lines forming voids (air gaps) between the metal lines (column 10, line 21).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the process of Uzoh to include air gaps in the second dielectric because Gaw illustrates that introducing air gaps is desirable because it results in the production of a chip with less capacitance delay and interconnect cross-talk. One of ordinary skill in the art would have been motivated to include air gaps in the second dielectric in order to obtain a faster chip.

14. As to claims 13, 15 and 17, Uzoh includes copper as a typical fill for copper lines (column 4, line 44), and Tantalum as a cap layer (column 4, line 65).

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mahmoud Dahimene whose telephone number is (571) 272-2410. The examiner can normally be reached on week days from 8:00 AM. to 5:00 PM..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Muhammad Dahimene
MD

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER